REMARKS

Claims 1 - 17 and 20 remain active in this application. Claim 18 - 19 have previously been canceled. Claim 1 has been amended to clarify novel aspects of the invention. New claims 21 and 22 have been added to more fully claim the subject matter considered to be the invention. Support for the amendments of the claims is found throughout the application, particularly in Figures 1, 8 and 9 and the description thereof on pages 6 - 10 and 12 - 14 and, in particular, page 10, lines 13 - 23. No new matter has been introduced into the application.

Amendment of the Title of the application ha been requested. It should be noted that the amendment requested conforms the Title to the Title as presented on the first page and abstract page of the application as originally filed. However, the word "storage" was additionally included in the original declaration and the error has persisted to date. If any other form of amendment is needed to carry out restoration of the original Title, an Examiner's Amendment is hereby authorized for such purpose, or, in the alternative, the undersigned would be please to present a supplemental amendment in any form as the Examiner may request.

Claims 1 - 12 and 20 have been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al. and Nikhil et al. Claim 13 has been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al., Nikhil et al. and Hartwell. Claims 14 - 15 have been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al., Nikhil et al. and Dwork et al. Claim 16 has been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al., Nikhil et al., Dwork et al. and Iwashita et al.

Claim 17 has been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al., Nikhil et al. and Seaman. Claim 19 been rejected under 35 U.S.C. §103 as being unpatentable over Irwin in view of Hartmann et al., Nikhil et al. in view of Gamo (sic - Reeve?). All of these grounds of rejection are respectfully traversed for the reasons of record and, particularly as being moot in view of the above amendments to claim 1.

In regard to the rejection of claim 19, it is respectfully pointed out that the stated ground of rejection is erroneous on its face since the rejection is based on a combination of references including Gamo while the discussion of the ground of rejection is otherwise silent in regard to Gamo but appears to rely upon Reeve, not included in the combination applied. In any event, this ground of rejection has been rendered moot by the cancellation of claim 19.

As noted in the "Background" section of this application, hardwired circuits capable of communication protocol conversion provide high speed of operation and throughput but cannot easily be modified to accommodate new protocols or changes in existing or developing protocols. General purpose processors can also be programmed to perform protocol conversion and can be easily re-programmed to accommodate new or changed protocols but have lower capacity and processing speed. The invention addresses these problems and achieves high throughput of data frames while performing protocol conversion by providing a plurality of processors in an architecture which can be dynamically reconfigured such that processors are operated in a combination of parallel and pipelined operations. By the above amendment, the previous recitation of "using parallel processing and pipelined processing" has been expanded to more clearly define the processor capabilities by which the parallel and

pipelined processing reconfiguration is preformed to accommodate extremely high (e.g. 10 Gb/sec) transmission bit rates. None of the prior art currently applied against the claims teaches or suggests anything approaching these functions or capabilities whether taken alone or in any combination.

It is recited in claim 1 that each processor of the plurality of processors includes a plurality of hardwired threads which are each capable of executing programs (including programs required for protocol conversion) in parallel within a given processor. Claim 1, as now amended, also recites that separate processors are pipelined using a high-speed interprocessor interconnect (which can be considered to be much in the nature of a cross-bar switch such that any input terminal/processor output can be connected to any output/processor input or interface) which serves to separate inbound signal processing from out bound signal processing and reduce processing load for a given processor by distributing inbound and outbound processing over respective processors. Thus, even at minimal processing loads, processing is performed in both parallel and pipelined operations as previously generally recited and now detailed.

Each processor is also capable of routing incoming data frames. In the invention, processing is expedited by directing incoming data frames which are related to data frames being processed by a given hardwired thread to that thread which expedites processing by eliminating or greatly reducing the need for memory accesses to determine context which will be common to related data frames as the data frames are processed in a pipeline fashion by that hardwired thread. Unrelated data frames are routed to a different hardwired thread on the same processor or a different processor and processed in parallel with the pipelined processing of other hardwired threads. Additional processors may be

invoked and data frames routed to them as the work queue of a given processor exceeds a threshold or when a free memory list is empty. Again, the routing can be performed at any processor based on workload conditions of that processor or memories of other processors which the processor can access and the determination of whether or not an incoming data frame is related or unrelated to other data frames being processed in that processor or particular other processors which expedites the placing and retrieving of pointers as well as directly routing a data frame to a particular other processor. Thus each processor can function to route data frames to balance workload in the system.

None of these features which are characteristic of the invention are taught or remotely suggested in the references applied. While Irwin discloses a multiprocessor system (and not for communication protocol conversion, as the Examiner admits), the architecture employs a master processor for routing by using a counter to direct data to different slave nodes for different procedural calls. This master/slave *processor* arrangement is also clearly distinct from a master *thread* for directing data frames to other processors or threads as they reach a given processor. Hartman et al. is cited only for the proposition, clearly derived through hindsight, that protocol conversion is a type of processing appropriate to Irwin. However, Hartmann teaches use of a "traffic circle" using a generic packet format for routing between processors and dedicated port adapters and not direct transfer of data frames between processors, as claimed. Nikhil, similarly, is cited only for teaching use of thread units and parallel and pipeline processing. The parallel and pipeline processing described in the passages of Nikhil relied upon by the Examiner appear to refer to operations performed on the threads, themselves or parallel operation of processors

to accommodate independence of threads using parallel four stage pipelines (see column 3, lines 24 - 30, following a passage relied upon by the Examiner, rather than any routing of data frames and, in any event, the threads or processors do not appear to be reconfigurable, particularly in response to data frame content, processor workload and memory state of other processors as data frames arrive at any processor. In summary, the basic combination of references applied to claims 1 - 12 and 20 appears to be substantially an attempted hindsight reconstruction of the invention which still fails to answer the explicit recitations of those claims even as finally rejected, much less as now amended. Nothing in any of the references taken singly or in any combination appears to even approach the concept of a system having an architecture which can reconfigure itself through data routing, much less based on both data content and workload and/or memory state of each processor as detected in any processor as now made clear by the above amendments.

The other references beyond the basic combination of Irwin, Hartmann and Nikhil similarly do not teach or suggest any of these features of the invention and do not mitigate the deficiencies of these references, in combination to answer the recitations of the claims or provide evidence of obviousness of any of the evident distinctions of the claimed subject matter therefrom. Hartwell is cited only for teaching use of a phase locked loop in an initialization/reset circuit.

Dwork et al. is cited for teaching rebalancing of workload among processors but apparently do so on the basis of deriving a consensus among the processors as to the state of completion of various tasks from time to time and reallocating the workload in response thereto. While all processors may be involved in doing so (as distinct from a master/slave arrangement such as Irwin) there is no reconfiguring the processors to

function in different parallel/pipeline configurations based on the content of incoming data or workload or memory conditions of any single processor. Iwashita et al. is cited by the Examiner for teaching monitoring of memory availability and halting receipt of incoming data when it exceeds memory capacity but does not appear to teach or suggest (and the Examiner does not assert otherwise or rely on it for teaching or suggesting) rerouting to another processor for processing in parallel, balancing of workload between processors or providing any other function of the invention for accelerating processing. Seaman is cited by the Examiner for teaching examination of bus activity but claim 17 to which it is applied, recites examination of the *interconnection resources of the plurality of processors* (e.g. the memory queues thereof - see the paragraph bridging pages 11 - 12 of the specification. Thus, it is clearly seen that the references do not support a conclusion of obviousness of the subject matter of the claims even as finally rejected, much less as now amended. That the Examiner has failed to make a *prima facie* demonstration of obviousness in regard to any claim is particularly evident from the Examiner's references to the teachings of various reference which do not correspond to the explicit recitations of the claims, particularly in combination or considered as a whole, as is required. Further, to the extent that Nikhil may teach both pipeline and parallel processing as the Examiner asserts, the invention has been clearly distinguished therefrom by expansion of that recitation to include particular configurations and relationships between threads and processors and between processors and the conditions under which the configuration is changed by data frame routing based on *both* data frame content and processor workload.

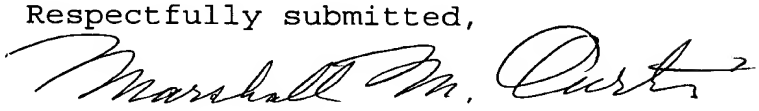
Accordingly, it is respectfully submitted that all

claims have been fully and patentably distinguished from the prior art the Examiner has applied and that the asserted grounds of rejection are clearly untenable, particularly in view of the above amendments. Therefore, reconsideration and withdrawal of the grounds of rejection of record is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

A petition for a one-month extension of time has been made above. If any further extension of time is required for this response and the concurrently filed Request for Continued Examination to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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